NANOSTONE PTE. LTD.

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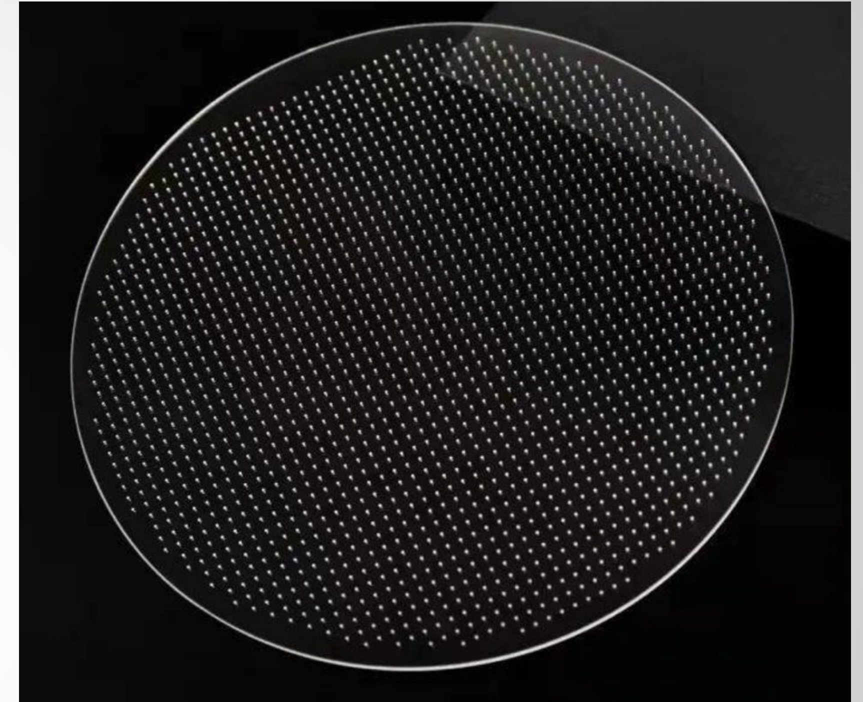
Silicon Wafer

Silicon Wafer Specification							
Diameter	2"	3"	4"	5"	6"	8"	12"
Grade	Test / Prime / Dummy						Dummy
Growth Method	CZ, FZ，FZ-NTD，FZ-GD						CZ
Orientation	< 1-0-0 > , < 1-1-1 >						<1-0-0>
Type/Dopant	P Type/Boron , N Type/Phos, N Type/As, N Type/Sb						P Type/Boron
Thickness (µm)	279	380	525	625	675	725	775
Thickness Tolerance	Standard ± 25µm, Maximum Capabilities ± 10µm						± 25µm
Resistivity	0.001 - 100 ohm-cm; 1,000-10,000 Ω•cm; >10,000 Ω•cm; >20,000 Ω•cm;						0.001 - 100 ohm-cm
Surface Finished	SSP/DSP						DSP
TTV (µm)	Standard < 10 um, Maximum Capabilities <5 um						Not Sure
Bow/Warp (µm)	Standard <40 um, Maximum Capabilities <30 um						Not Sure
Particle	<10@0.3µm / <10@0.2µm						Not Sure

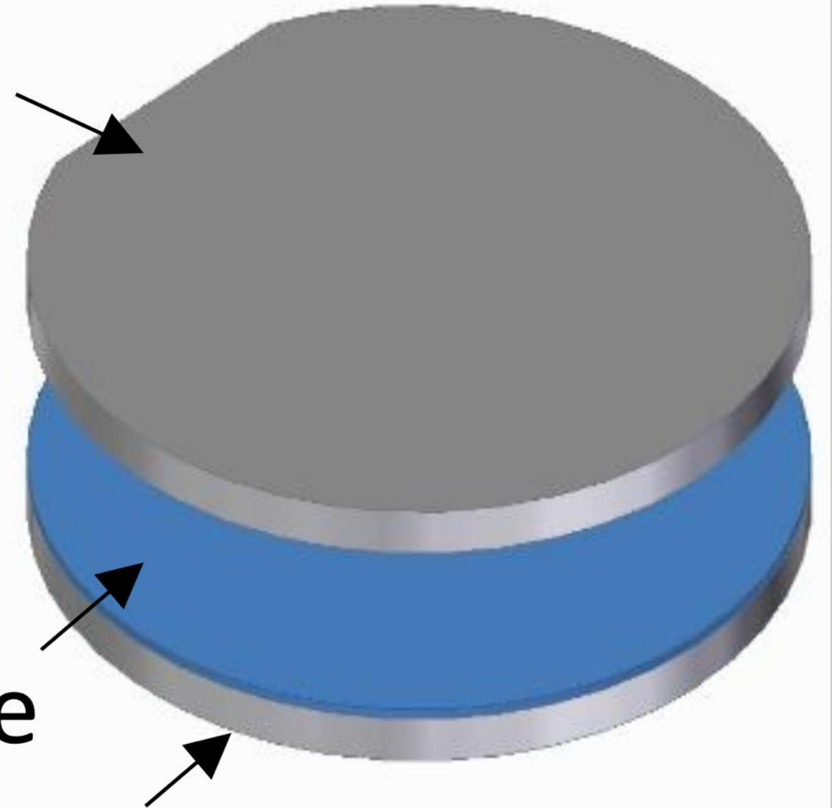
Glass Wafer

Parameter	Standard Specification
Materials	**Fused Silica** JGS1/JGS2/JGS3, **SCHOTT,** Borofloat33, D263t, B270i, **Corning,** 7980, Eagle XG, etc.
Diameter	2”, 3”, 4”, 6”, 8”, 12” and Square
Thickness	0.1-3.0mm
TTV	Standard < 10 um, Maximum Capabilities <1 um
Bow	Standard < 30 um, Maximum Capabilities <30 um
Warp	Standard < 30 um, Maximum Capabilities <30 um
Surface	DSP, SSP
Roughness (Ra)	Standard Ra< 1nm, Maximum Capabilities <0.5nm
S/D	Standard 60/40, Maximum Capabilities 20/10
Remark	Customized is available



SOI Wafer

Parameter	Parameter	4", 5", 6", 8"	Parameter
Device layer	Type	P, N	Device thickness >1.5um Tolerance ± 2-5um
	Resistivity	0.001~10000 ohm-cm	
	Orientation	<100>,<110>,<111>	
	Thickness	>1.5 um	
	Tolerance	+/- 0.5 um	
BOX	Thickness	0.2~4.0 um	Grown on Handle, Device
	Uniformity	+/-5%	or Both wafers
Handle layer	Type	P, N	Handle thickness 200-1100um Tolerance ± 5-10um
	Resistivity	0.005~10000 ohm-cm	
	Orientation	<100>,<110>,<111>	
	Thickness	200~1000um	
	Tolerance	+/- 5 um	

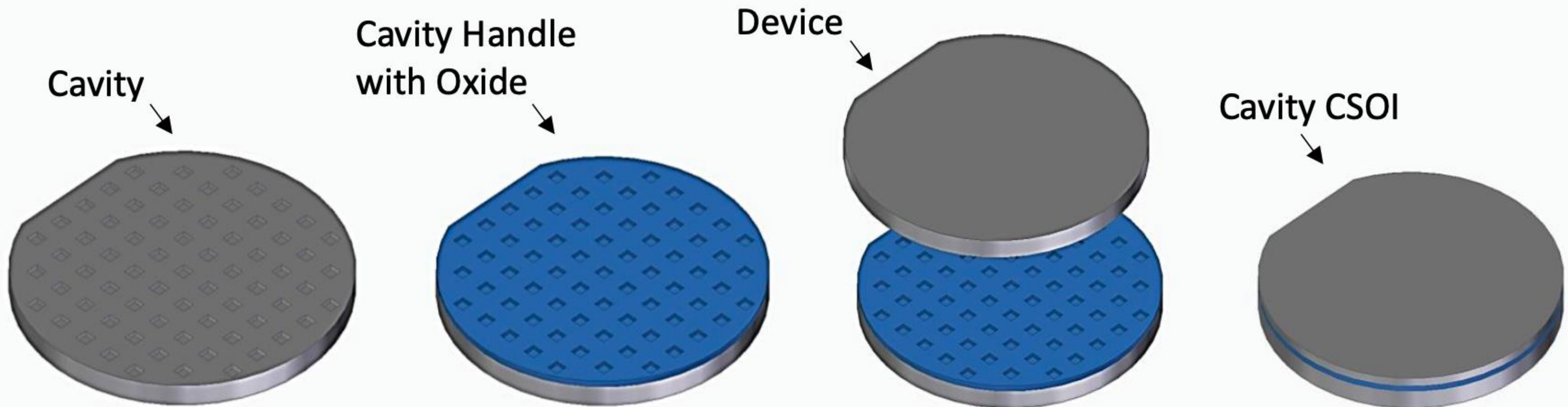


Cavity SOI

Membrane Thickness/SOI Thickness	>2 um
Membrane Tolerance	+/-0.5 um
Cavity Span: Membrane Thickness	<50:1 um (dependent on design)
Minimum Bonding Size Features	20 um
Alignment Accuracy of Cavity to Alignment Marks	+/-3 um
Cavity Depth	1-30 um @ +/-10%31-300 um @ +/-20%
Cavity Location	Handle,Device or Buried Oxide

Appication:

- Advanced pressure sensors
- Inertial MEMS
- Microfluidics
- Resonators
- Microphones

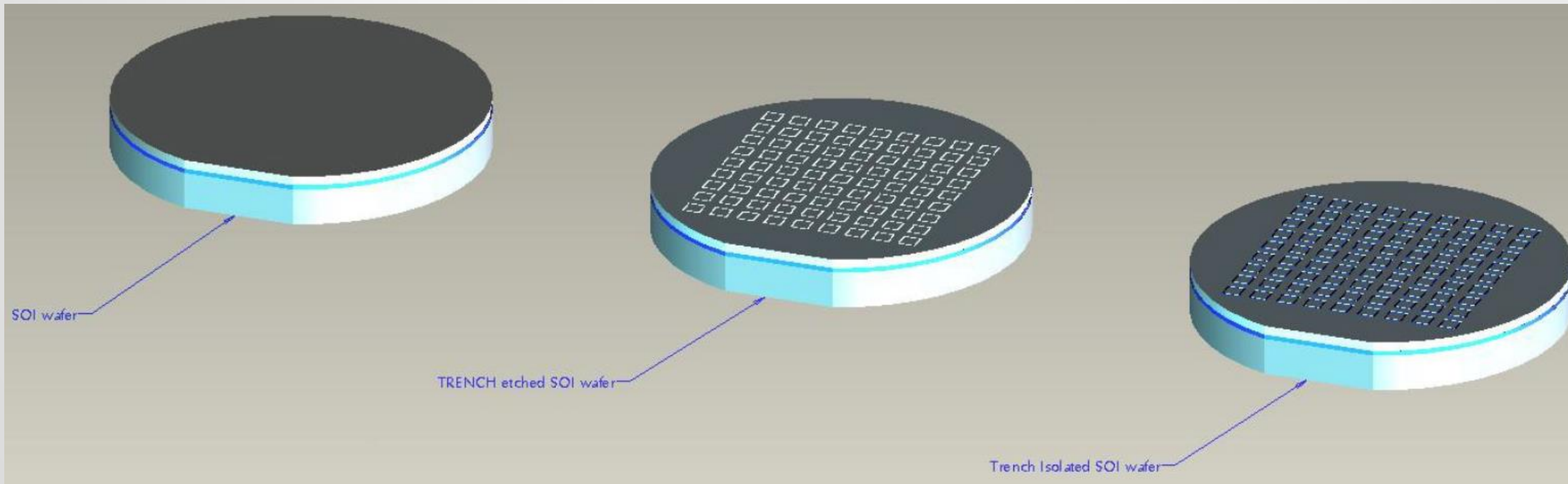


Trench SOI

Trench Mask tone	Positive resist
Trench Mask type	E-beam master for projection aligner
Trench line width	>2um
Trench Aspect ratio	15:01
Trench Sidewall doping type	Phosphorus & Boron
Trench refill - oxide (eachsidewall)	0.1 -1.0 um
Trench refill- polysilicon	To fill (Doped or undoped Polysilicon)
Planarisation	CMP
Final field oxide	Thermal oxide + TEOS up to 2.0 um

Applications

- MEMS devices
- Solid State Relay photovoltaic generators
- Photovoltaic cells and Optoelectronic devices/ICs
- High Voltage Analog ICs for telecommunications
- High performance bipolar circuits
- Smart Power ICs
- Integrated Sensors



EPI Wafer

Parameter	Silicon Epi wafers	Silicon on Sapphire Epi wafers
Diameter	76, 100, 150, 200 mm	76, 100, 150 mm
Substrate Orientation	(111), (100)	R-plane
Substrate dopant	Antimony, Boron, Arsenic	-
Epi-layer thickness, µm	1,0 – 150	0,3 – 2,0
Epi-layer dopant	Phosphorous, Boron, Arsenic	Phosphorous, Boron
Epi-layer resistivity, Ohm.cm N-type P-type	0,005 – 1500 0,005 – 1500	acc. to spec. 1,0 - 0,01
Multi-layer structures	Up to 4 layers	1 layer
Buried layer epitaxy	Up to 3 buried layers (p^+, n^+)	-

Semi-insulated SiC Substrate

Parameter	Standard Specification		
Grade	Production	Research	Dummy
Polytype/ Surface orientation on-axis/ Surface orientation off-axis	4H/<0001>/0±0.25°		
FWHM	≤45arcsec	≤60arcsec	≤100arcsec
Diameter/Thickness/Notch Orientation/Notch Depth/Si-face Roughness	200±0.2mm /500±25μm/[1-100]±5°/1~1.5mm/Ra≤0.2nm		
Resistivity	≥1E8Ω•cm	100% area>1E5Ω•cm	70% area>1E5Ω•cm
LTV	≤5μm(10mm*10mm)	≤10μm(10mm*10mm)	≤15μm(10mm*10mm)
TTV	≤10μm	≤15μm	≤20μm
Bow	-25μm~25μm	-45μm~45μm	-65μm~65μm
Warp	≤35μm	≤50μm	≤70μm
Micropipe density	≤2ea/cm2	≤10ea/cm2	≤50ea/cm2
Metal impurities	≤5E12atoms/cm2		NA

N-type SiC Substrate

Parameter	Standard Specification		
Grade	Production	Research	Dummy
Polytype/ Surface orientation tolerance	4H/4°toward<11-20>±0.5°		
Type/Dopant	N-type/Nitrogen		
Diameter/Thickness/Notch Orientation/Notch Depth/Si-face Roughness	200±0.2mm /500±25μm/[1-100]±5°/1~1.5mm/Ra≤0.2nm		
Resistivity	0.015~0.025Ω•cm	0.01~0.03Ω•cm	NA
LTV	≤5μm(10mm*10mm)	≤10μm(10mm*10mm)	≤15μm(10mm*10mm)
TTV	≤10μm	≤15μm	≤20μm
Bow	-25μm~25μm	-45μm~45μm	-65μm~65μm
Warp	≤35μm	≤50μm	≤70μm
Micropipe density	≤2ea/cm^2	≤10ea/cm^2	≤50ea/cm^2
Metal impurities	≤5E12atoms/cm^2		N/A
TSD	≤500ea/cm^2	≤1000ea/cm^2	N/A
BPD	≤2000ea/cm^2	≤5000ea/cm^2	N/A
TED	≤7000ea/cm^2	≤10000ea/cm^2	N/A

Sapphire Wafer

Parameter	Standard Specification	
Growth Method	KY	
Size	2”	4”
Tol(±)	<0.25 mm	
Thickness	430±25mm	650±25mm
Material	AL2O3>99.995%	
Orientation	C Plane [0001] to M (1-100) 0.2°±0.1°;	
Flat	16±1mm at C-plane [0001] to M-plane (1-100) 0.2° ±0.1°	30±1 mm at A-plane (11-20) ± 0.2°
Frontside Ra	＜0.3 nm(Epi ready polished)	
Backside Ra	＜1.2 nm(As lapped or fine ground)	
TTV	＜10um	
Bow	＜15um	
Warp	＜20um	
Particle	No quest	
Appearance	transparency	

LiTaO3 wafers(White or Black)

Parameter	Standard Specification	
Curie Temp	603±2.0℃	
Cutting Angle	X/Y/Z etc	
Diameter/Size	2”/3”/4”LT wafer	
Tol(±)	<0.20 mm	
Thickness	0.1～0.5mm or more	
Primary Flat	16mm/22mm/32mm	
TTV	<3μm	
Warp	<40μm	
Surface Type	Single Side Polished /Double Sides Polished	
Polished side Ra	<0.5nm	
Back Side Criteria	General is 0.2-0.5μm or as customized	
Edge Criteria	R=0.2mm or Bullnose	
Optical doped	Zn/MgO etc	
Wafer Surface Criteria	Contamination,	None
	Particles C>0.3μ m	<=30
	Scratch,Chipping	None

LiNbO3 wafers(White or Black)

Parameter	Standard Specification	
Curie Temp	1142±2.0℃	
Cutting Angle	X/Y/Z/Y36/Y41Y64/Y128/etc	
Diameter/size	3”/4”/6"LN wafer &8"under R/D	
Tol(±)	<0.20 mm	
Thickness	0.1～0.5mm or more	
Primary Flat	22mm/32mm/42.5mm /57.5mm	
LTV(5mmx5mm)	<1μm	
TTV	<3μm	
BoW	-30<bow<30	
Warp	<40μm	
PLTV(<0.5um)	≥95%(5mm*5mm)	
Orientation Flat	All available	
Surface Type	Single Side Polished /Double Sides Polished	
Polished side Ra	<0.5nm	
Back Side Criteria	General is 0.2-0.5μm or as customized	
Edge Criteria	R=0.2mm or Bullnose	
Wafer Surface Criteria	Transmissivity	general:5.9x10-11<s<2.0*10-10 at 25℃
	Contamination	None
	Particles C>0.3μ m	<=30

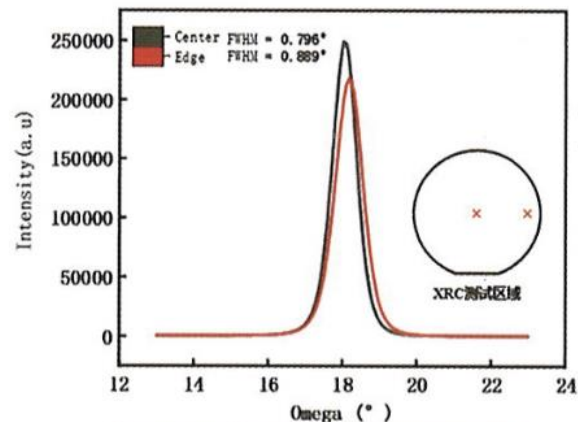
GaAs Substrate

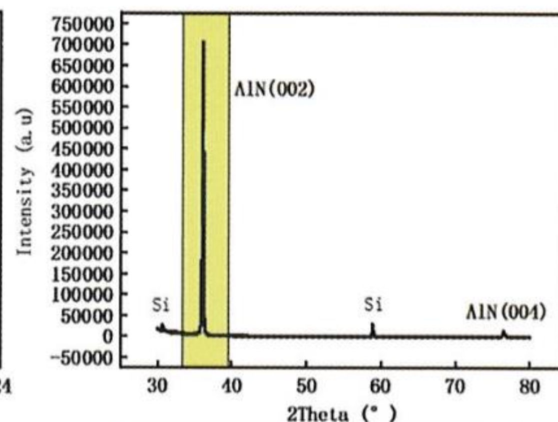
Parameter	Standard Specification	
Grade	Prime	Mechanical
Diameter	150±0.25mm	150±0.3mm
Growth Method	VGF	
Type/Dopant	N-type/Un	
Orientation	(100)2°off toward<110>±0.5	
Notch Orientation	(010)±2°	
Notch Depth	1+0.25mm/90+5/-0°	(1-1.25)mm 89°-95
Resistivity	≥1.0E8Ω•cm	>1.0E7Ω•cm
Mobility	＞4500cm2/v.s	N/A
EPD	Ave.≤10000/cm^2	<10000/cm^2
Thickness	675±25μm	
TTV/TIR/Bow/Warp	≤4/≤4/≤4/≤5μm	≤15/≤15/≤15/≤15μm
LTV	≤1.0um @20mm*20mm,PLTV≥90% μm	N/A
LFPD	≤1.0um @20mm*20mmPLFPD≥90% μm	N/A
Edge Rounding	0.25mmR	N/A
Particle	≤120/wafer@0.3um^2	N/A
Surface Finish	P/P	
Package	Cassette	

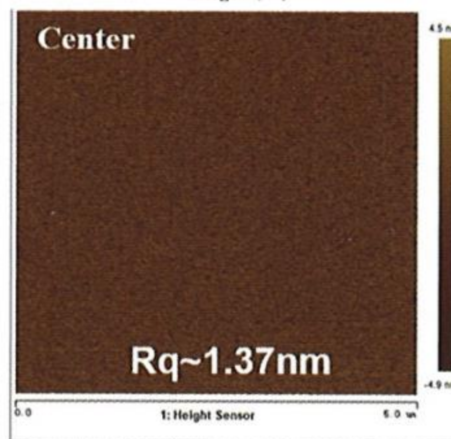
硅基氮化铝 (AIN on Si)

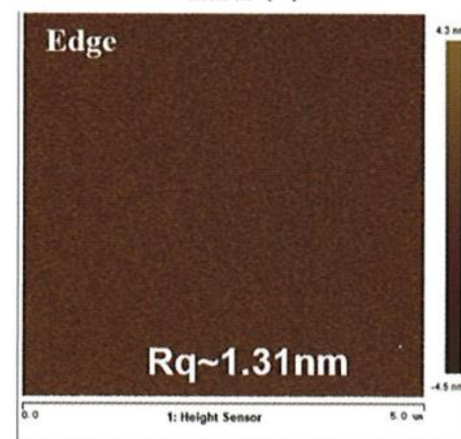
硅基氮化铝 (AIN on Si)

产品名称	AIN on Si
基底材料(Substrate)	500±10μm Si(111)
直径(inch)	2inch、4inch……可定制
AIN外延厚度 (Thickness)	50nm-1μm
晶面取向 (Orientation)	c-aixs [0001]
表面粗糙度(nm)(5x5μm)	Rq< 1.5nm (200nm)
XRC (°)@ (0002)	<0.9° (200nm)
总厚度变化(TTV)	<7μm
翘曲度(Warp)	<30μm
弯曲度(Bow)	-10~15μm





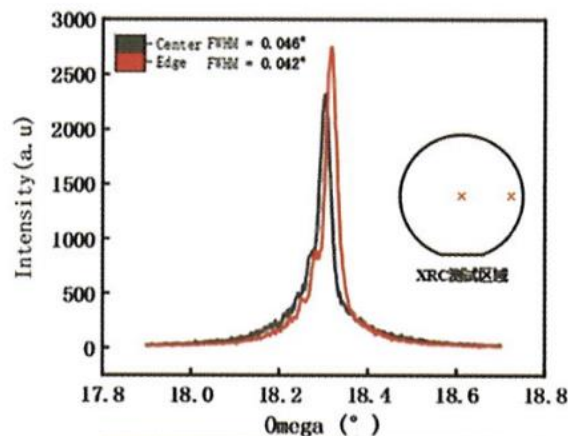


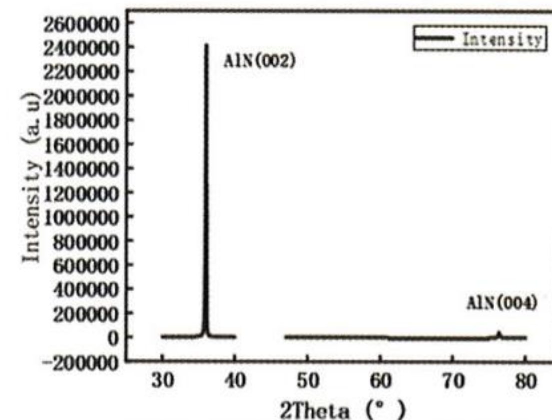


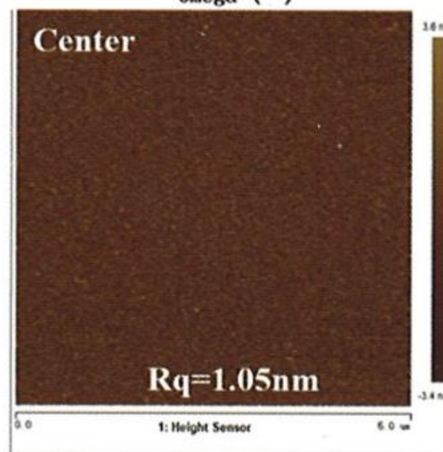
蓝宝石基氮化铝(AlN on Sapphire)

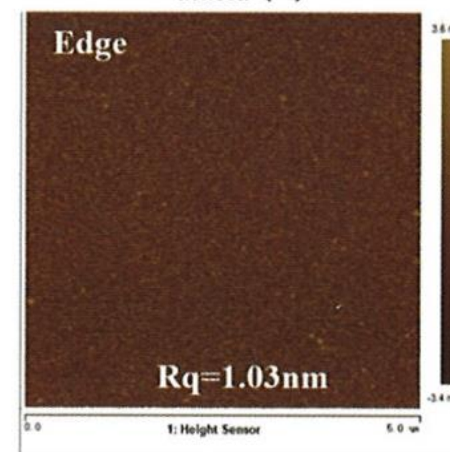
蓝宝石基氮化铝 (AlN on Sapphire)

产品名称	AlN on Sapphire
基底材料(Substrate)	430-440μm Sap(002)
直径(inch)	2inch、4inch......可定制
AlN外延厚度 (Thickness)	50nm-1μm
晶面取向 (Orientation)	c-aixs [0001]
表面粗糙度(nm)(5x5μm)	Rq< 1.20nm (200nm)
XRC (°)@ (0002)	<0.05° (200nm)
总厚度变化(TTV)	<7μm
翘曲度(Warp)	<30μm
弯曲度(Bow)	-10~15μm





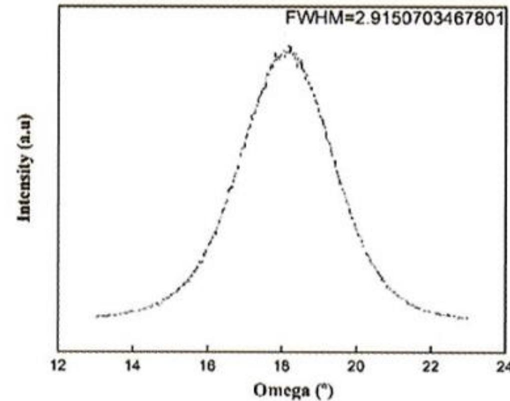




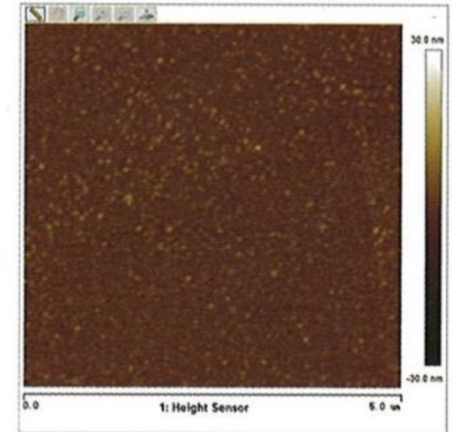
金刚石基氮化铝(AlN on diamond)

金刚石基氮化铝 (AlN on diamond)

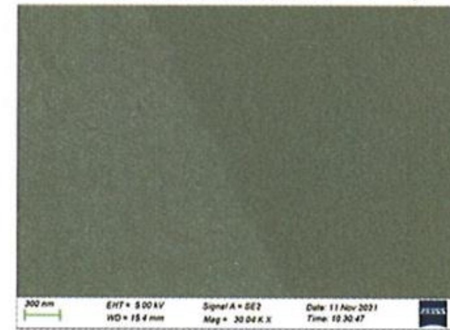
产品名称	AlN on diamond
基底材料(Substrate)	200 μm~500 μm; 多晶金刚石
直径(inch)	2inch……可定制
AlN外延厚度 (Thickness)	50nm-1 μm
晶面取向 (Orientation)	c-aixs [0001]
表面粗糙度(nm)(5x5μm)	Ra < 2nm (200nm)
XRC (°)@ (0002)	<5° (200nm)
总厚度变化(TTV)	＜30 μm（2 inch）
翘曲度(Warp)	＜300 μm（2 inch），可定制
平面度(PV)	＜15fringe（Ø20mm）



金刚石基氮化铝 (0002)XRD摇摆曲线
(FWHM约为2.915°)



金刚石基氮化铝AFM形貌图
(Ra:1.74-2.84nm)



氮化铝薄膜SEM图(50K)

Please feel free to contact us!!
Email: daniel@nanostone.sg
Phone: +65 98267050 (WhatsApp and wechat)

Thanks